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A/D CONVERSION: A DIGITAL VOLTMETER

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NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

A/D CONVERSION: A DIGITAL VOLTMETER

by

Mehmet Deniz Celbiş

Thesis Advisor: R. Panholzer

December 1973

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A/D Conversion: A Digital Voltmeter

by

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Lieutenant Junior Grade, Turkish Navy
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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1973

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ABSTRACT

During the past few years, advancement of the integrated circuit technology yielded medium and large scale integration of commonly used electronic circuitry.

One of the special MSI devices commercially available today is the Fairchild 3814 Digital Voltmeter Logic Array which contains most of the logic required for a 4 1/2 decade digital Voltmeter.

In this thesis the design of an inexpensive four digit, auto-scaling digital voltmeter is presented with results of tests performed on this meter.

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I. INTRODUCTION

A familiar method of analog-to-digital conversion in digital voltmeters is ramp-comparator analog-to-time conversion utilizing an electronic integrator. A sample-and-hold network samples the unknown voltage and holds this value. The integrator then integrates either a positive or negative reference voltage. The time for the integrator to reach the value stored in the sample-and-hold circuit is proportional to the unknown voltage. The number of clock pulses proportional to this time are counted for digital readout.

This method though simple and inexpensive, suffers from several disadvantages. To maintain accuracy, a highly stable clock oscillator is required. Also, any practical system will have noise added to the input signal, and the sample-and-hold circuit may hold a noise peak. Components must be very precise and the switching scheme must not change the value of the voltage stored in the sample-and-hold circuit.

A second method of ramp-comparator conversion utilizes an electronically resettable integrator. The integrator is reset to a value proportional to the unknown voltage plus a positive bias. The integrator integrates a reference voltage until it reaches a predetermined level set by a precision limiter. This time is again proportional to the unknown voltage. The use of the positive bias has the advantage that the integrator always integrates the same

polarity of reference voltage for either polarity of input signal, thus eliminating complex switching circuitry. The precision limiter also yields very accurate limiting. This method still requires a highly stable clock, and the integrator can still be reset to a noise peak rather than a true value.

A third method of ramp comparator conversion is known as dual slope integration. This method will be described in more detail in this section. It will be shown that any long term drift in the clock frequency has no effect. The dual slope method does not require a sample-and-hold network because the input signal is integrated to determine the unknown value. A disadvantage of this method is the complex polarity switching circuit required. Such switching was not attempted in this thesis.

The purpose of this project was to build an inexpensive digital voltmeter incorporating the best features of the conversion methods previously described. The dual slope technique was utilized to avoid the effect of drift in the clock frequency. Since the input signal was integrated in determining the unknown voltage, high frequency noise effects were reduced.

A special zero-level determining circuit was used to prevent false triggering of the digital portion of the device.

II. DUAL SLOPE INTEGRATION

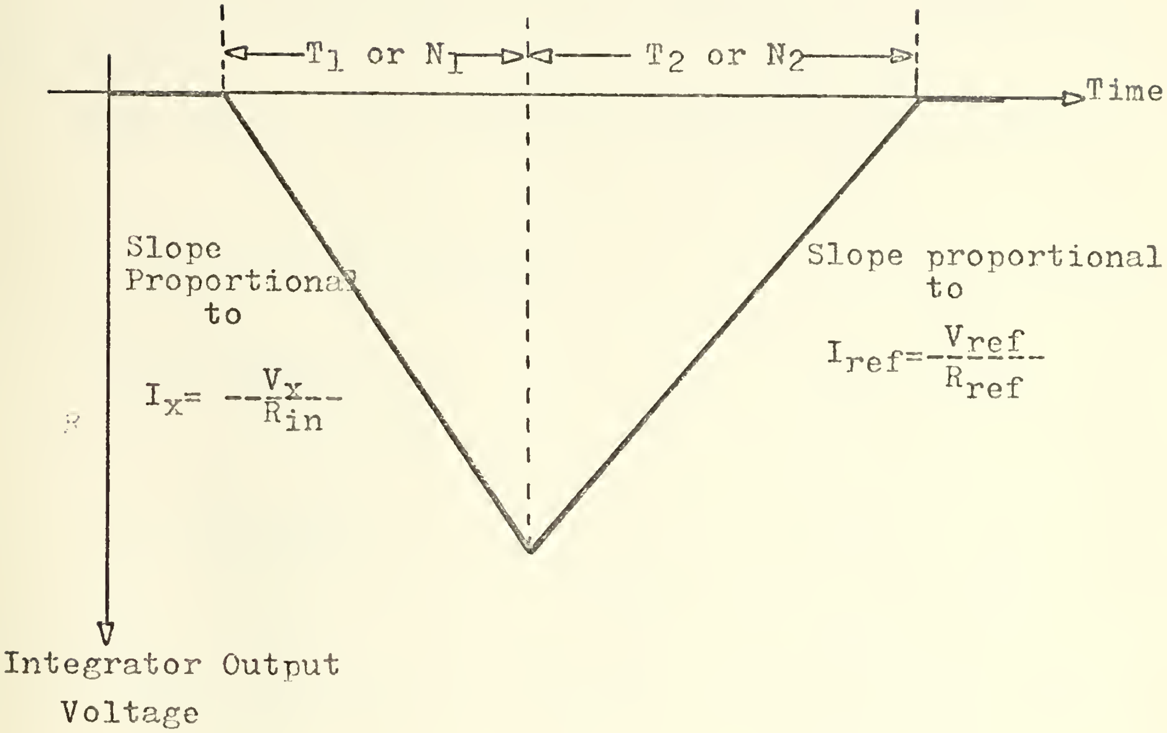

T1 or N1
T2 or N2
Time
Slope Proportional to
$I_x = -\frac{V_x}{R_{in}}$
Slope proportional to
$I_{ref} = -\frac{V_{ref}}{R_{ref}}$
Integrator Output Voltage

Figure 1. Dual Slope Integration

Dual slope integration is a two step "analog to time" (A/T) conversion technique, as illustrated in the waveform in Figure 1. The integrator is initially at a zero level. At the beginning of a sample period, the integrator begins to integrate down with a slope proportional to the unknown voltage V_x. The integrator continues to integrate for a fixed amount of time T_1, determined by the digital portion

of the circuit. At the end of this time the integrator input is switched to a negative reference current I_{ref}, so that the integrator commences integration back up until it returns to the zero level. At this point, a precision comparator changes states signalling that the integrator has crossed the null point. The integrator is subsequently set to zero.

From Figure 1, the following equations can be written:

$$K_1 I_x T_1 = K_2 I_{ref} T_2 \qquad (1)$$

$$T_2 = \frac{K_1 T_1}{K_2 I_{ref}} I_x$$

$$K = \frac{K_1}{K_2 I_{ref}}$$

$$T_2 = K T_1 I_x \qquad (2)$$

Since the number of pulses counted during each integration step equals the product of time and repetition rate, the number of pulses counted during the second integration step is:

$$N_2 = K N_1 I_x \qquad (3)$$

where N_1 is the number of pulses allowed for the first integration. If there had been a percent drift, Δ, in the clock frequency N_2 would take the form;

$$N_2 \Delta = K N_1 \Delta I_x \qquad (4)$$

which is the same as equation (3); this demonstrates the advantage of this technique. The effect of long term drift in the clock frequency has been avoided. No crystal oscillator was required since it was only necessary that the frequency of the clock be constant during each sample period to maintain accuracy.

III. FUNCTIONAL BLOCK DIAGRAM

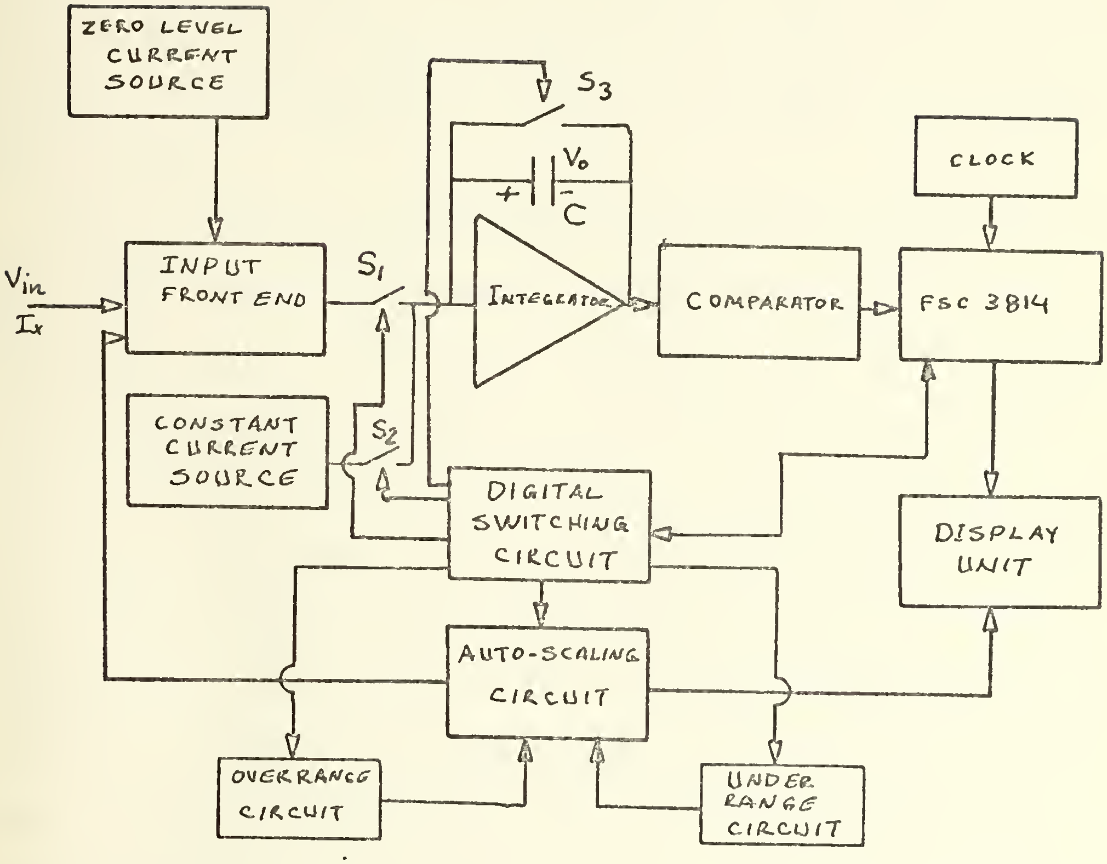


Figure 2. The Functional Block Diagram of the Digital Voltmeter

The block diagram consists of an input front end, a constant current source, a zero level current source, an integrator, a comparator, a clock, the 3814 digital voltmeter array, a digital switching circuit, an auto scaling circuit, overrange and underrange circuits and a display unit.

At the beginning of each sample period ($T = T_o$), switch S_1 is closed; S_2 and S_3 are open. The integrator integrates the unknown current, which is proportional to V_x, until time T_1 or a fixed number of clock pulses has been delivered by the digital circuit. At that time capacitor C has been charged by current I_x to a value of V_o volts. The integrator output is then negative. At time T_1, switch S_1 is opened and S_2 is closed.

The integrator is subjected to I_s, the current from the constant current source which causes the slope of the discharge curve of C to be a constant. The output voltage of the integrator crosses the zero level, the comparator shifts states, signalling the 3814 to latch the value of its counters. The number of clock pulses counted during time T_2, which is proportional to the time required for the integrator to reach zero level, is proportional to the unknown voltage. Switch S_2 is then opened, S_1 and S_3 are closed, and the integrator is reset to its zero level, marking the beginning of a new sampling period.

Display is held until the end of the subsequent sampling period. Since all switching and timing is controlled by the digital circuit, it is discussed first.

IV. CIRCUIT DESCRIPTION

A. FAIRCHILD 3814 DIGITAL VOLTMETER LOGIC ARRAY

The 3814 provides the logic required to implement a 4½ decade digital voltmeter. In addition to four full decade counters and two overflow latches, the device is designed to drive a multiplexed display providing a Binary Coded Decimal output (to drive a BCD Converter) and five decoded outputs to strobe the display.

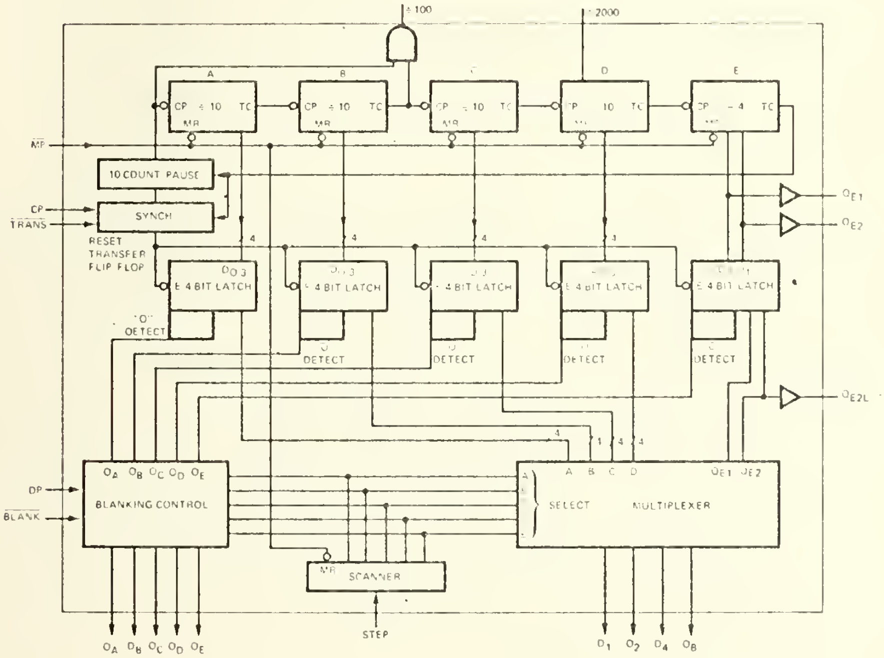


Figure 3. Block Diagram of the 3814

As seen from Figure 3, the 3814 is clocked by the CP input and provides 4½ decades of BCD counts, with a modulus of 40,000. The second decade's output was made available to provide a pulse for every 100 input clock pulses ("divide-by-100" output). The output of the first flip-flop (the "thousands" decade) is buffered and brought directly off the chip as "divide-by-2000" output. The outputs of both flip-flops of the fifth "half decade" are available as outputs Q_{E2} and Q_{E1}. The latched state of the most significant bit (Q_{E2L}) was also made available.

A sampling period starts when the counters of the 3814 are at 30,000. The 3814 then counts an additional 10,000 clock pulses, at which time it is in the 00,000 state. At this count the device ignores the next 10 clock pulses, still remaining in 00,000 state. This pause is used to accomplish the necessary current switching as described in Section III and to avoid transients which might cause false triggering of the comparator.

Following the 10 count pause, the counters in the 3814 resume counting the clock pulses until signaled by the comparator. The comparator generates a TRANSFER command for this purpose. The TRANSFER command causes the 3814 to latch and make available the count stored in the counters. This count is proportional to the measured voltage. If no TRANSFER command was generated, counters would go on counting until they reach 39,999 and the cycle would be repeated. Only one

transfer command is accepted during the interval 00,000 to 39,999 to prevent false triggering.

The state of one of the 4½ decade counters is presented as a BCD multiplexed output (Q_1, Q_2, Q_4, Q_8). One of the five decoded outputs, (O_A, O_B, O_C, O_D, O_E) goes to HIGH, indicating which decade's count is present at the BCD output of the multiplexer.

The blanking input ($\overline{\text{BLANK}}$) is used to prevent interference while the output of the 3814 is being multiplexed. The scanner input signal (STEP) was applied to the blanking input to assure that the segment select inputs are stable prior to the digit select inputs.

The decimal point input (DP) is for leading zero suppression. This input was derived by the auto-scaling circuit in order to blank the most significant digit, when a count such as $01.2\dot{3}$ was displayed.

The count state of the 3814 is made available by the states of the two overflow flip-flops, Q_{E2} and Q_{E1}. Q_{E1} is the least significant bit (LSB), while Q_{E2} is the most significant bit (MSB) of decade 5. The fifth decade is a half decade and consists of only two flip-flops or two bits of information. Since there are four "÷ 10" blocks prior to the fifth decade, this decade will change its state at every 10,000 count. The count state of the 3814 is monitored as shown in Table 1.

PERIOD	COUNT	Q_{E2}	Q_{E1}
A	00,000 to 9,999	0	0
B	10,000 to 19,999	0	1
C	20,000 to 29,999	1	0
D	30,000 to 39,999	1	1

Table 1. States of Q_{E1} and Q_{E2}

These Q_{E1} and Q_{E2} outputs are decoded and used for switching and synchronization in the analog circuit.

B. CLOCK CIRCUIT

In order to obtain a reasonably stable and noise free clock, a dual retriggerable, resettable monostable multivibrator, (Fairchild 9602) was used. The frequency and the accuracy of the 9602 is a function of the external timing components and has excellent immunity to noise on the V_{cc} and ground lines. The Logic Diagram is shown in Figure 4.

With a clock frequency of 600 kHz, the unknown input voltage is integrated for 1.667×10^{-2} seconds or 10,000 clock pulses. This time duration corresponds to "period D" of Table 1. One measurement period lasts for 6.667×10^{-2} seconds or 40,000 clock pulses. The period of the clock, t_w, is controlled by R_1C_1 and is given by:

$$t_w = 0.31\ R_1C_1\ (1 + \frac{1}{R_1}).$$

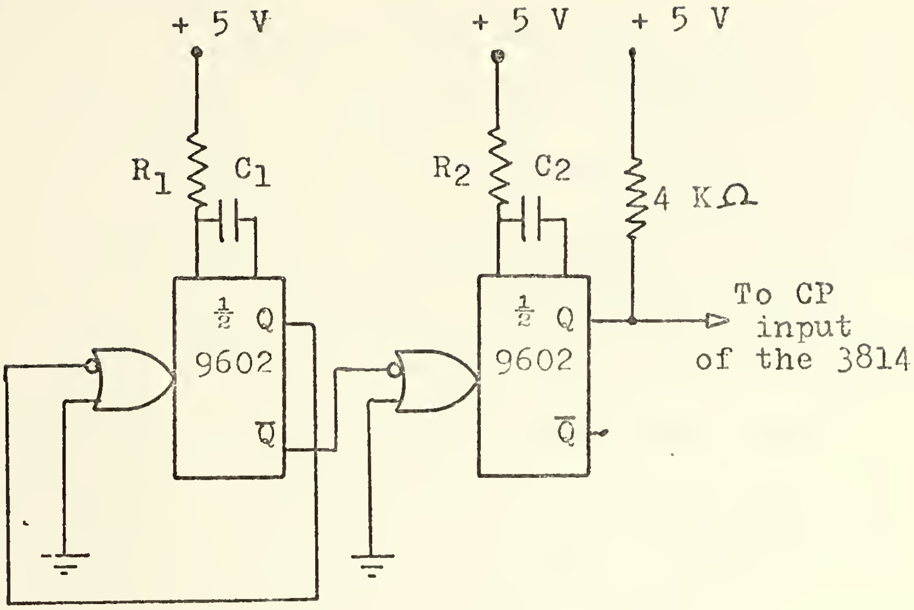


Figure 4. The Logic Diagram of the 9602

The selected clock frequency has a period of 1.667×10^{-6} seconds. In order to obtain the desired period, an R_1 of 13.78 KΩ and a C_1 of 390 pF was chosen. A pulse duration of 4.2×10^{-5} seconds was obtained by setting R_2 equal to 20 KΩ and C_2 equal to 68 pF. In the actual circuit, 20 KΩ potentiometers were used for both R_1 and R_2 and were adjusted to obtain the desired frequency. A "pull-up" resistor of 4 KΩ was used at the clock output to insure proper logic levels. External components were kept as close as possible to the 9602 chip and a 10 μF electrolytic capacitor was used

between V_{cc} and ground to eliminate noise which occured in the actual circuit after construction.

C. DISPLAY CIRCUIT

As presented in Section IV-A, the count state of the 3814 is latched into five latches when a TRANSFER command is received and the BCD outputs of these latched values are fed into an output circuit, which consists of a multiplexer, blanking control and a scanner. The scanner requires a STEP input which directly controls the multiplexing action. At each STEP pulse, a BCD output of one digit appears at the output leads of the multiplexer (O_1, O_2, O_4, O_8), while one output of the blanking control is HIGH, indicating which decade's count is present at the BCD outputs.

For the display, four Fairchild FND 70 single digit LED numeric displays were selected. The FND 70 is a seven segment plus decimal point display.

In order to decode the BCD outputs of the 3814 into seven segments, a Fairchild 9368 TTL/MSI, 7 segment decoder/driver was used. The 9368 eliminates the need for drivers and pull-up resistors normally required for LED displays and directly interfaces with the FND 70. The 9368 is capable of supplying 19 mA to each segment of the FND 70. In this application, all FND 70 LED display segment inputs are connected in parallel to the output of one 9368 chip, but ground returns of each digit is switched ON and OFF by a high-βdc transistor (MPS 6562). The digit select outputs of the 3814 (O_A, O_B, O_C, O_D, O_E) are HIGH when a BCD output is present, and

can supply only 200 μA. This is not enough base current to saturate the MPS 6562 switching transistors. Therefore, a suitable buffer (TTL/SSI 7438 quad 2-input nand buffer) was used.

In this application only four of the five available digit outputs of 3814 were used. The accuracy of the fifth digit was considered meaningless with the components used in the analog circuitry. Four FND 70 seven segment LED displays, one 9368 seven segment/driver, one 7438 nand buffer and four MPS 6562 high-β_{dc} transistors constitute the display circuit, except for the decimal point circuit. The block diagram of the display circuit is shown in Figure 5.

As multiplexing input to the 3814 scanner, the "÷ 100" output of the 3814 was used. This resulted in a scanning rate of 600 Hz with a duty cycle of 20% which provided a bright display.

D. LEVEL DETECTOR (COMPARATOR)

The functional block diagram in Section III describes the comparator as the final stage of the analog portion of the circuit. The comparator acts as a level sensor with hysteresis. The input and output curves of the comparator are shown in Figure 6.

When the comparator senses the zero level crossing of the integrator output, it shifts states from HIGH to LOW, which signals the digital circuit. This signal is the $\overline{\text{TRANSFER}}$ input to the 3814. In order to obtain precise zero

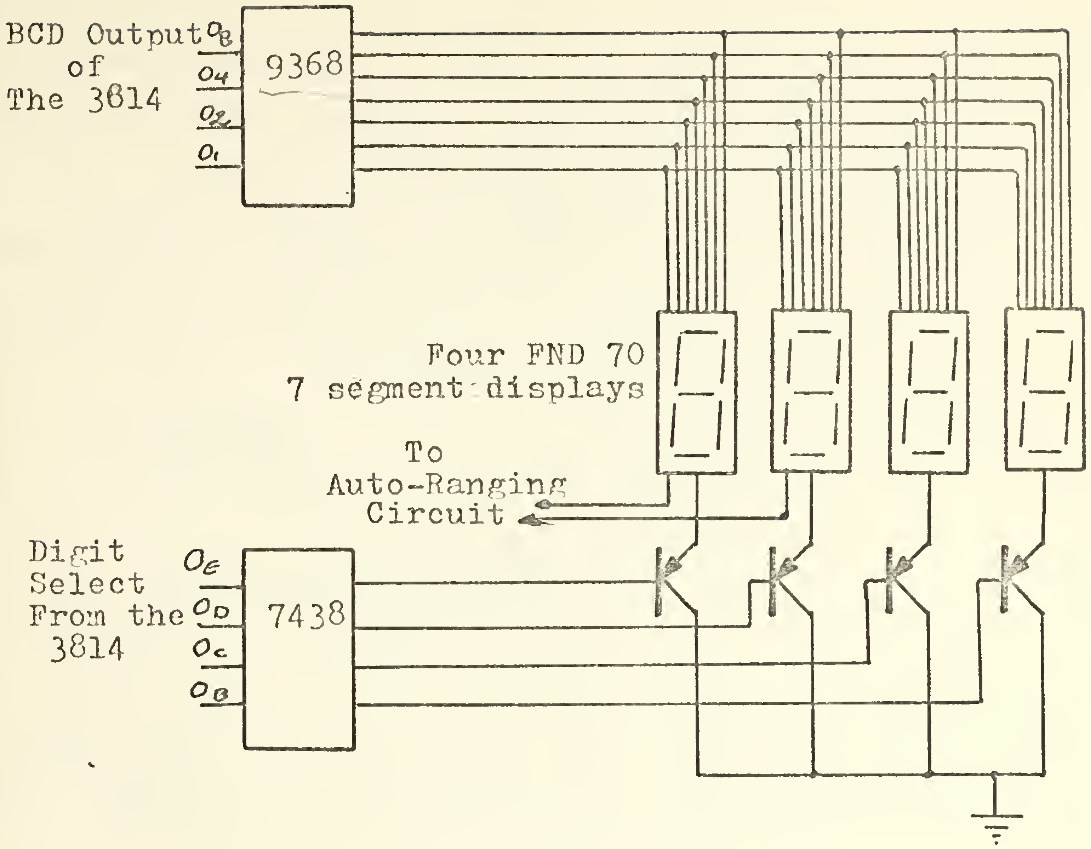


Figure 5. The Display Circuit

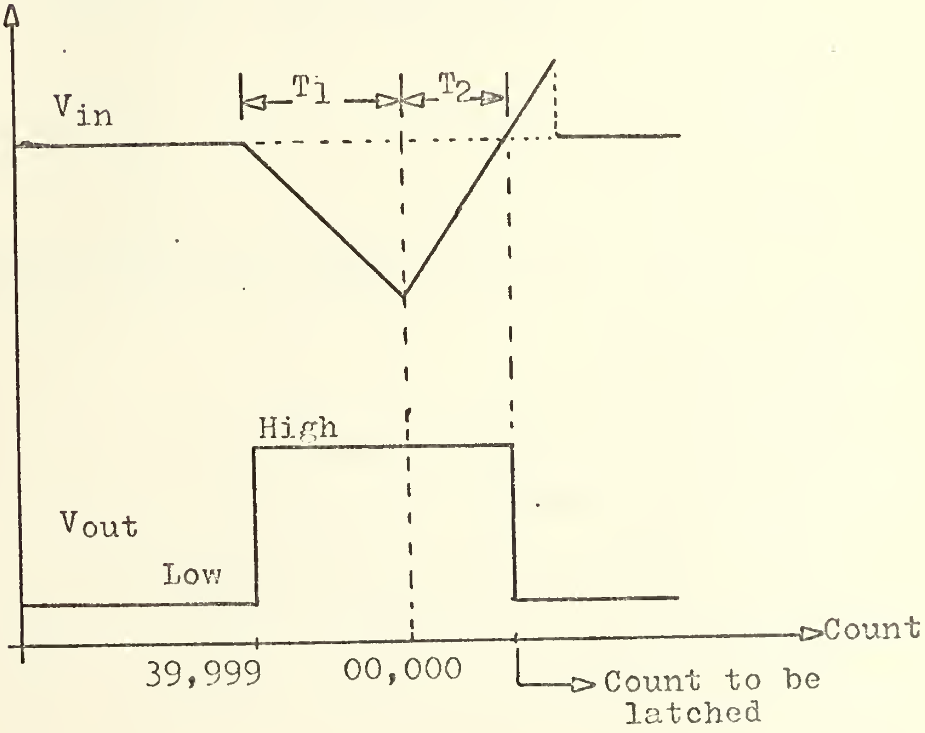


Figure 6. Input and Output of the Comparator

level crossing sensing, a μA 734 precision voltage comparator was used as shown in Figure 7. In order to sense the level precisely, hysteresis voltage V_{HYS}, and offset voltage must be kept as small as possible. Formulas 5 and 6 give the relations of R_1 and R_2 for this purpose.

$$R_s = \frac{R_1 R_2}{R_1 + R_2} \qquad (5)$$

$$V_{HYS} = \frac{R_1 (V_o \text{ MAX} - V_o \text{ MIN})}{R_1 + R_2} \qquad (6)$$

V_o(MAX) must be + 5V for the 3814 interface, and V_o(MIN) = 0,2V. Selecting R_1 = 100Ω and R_2 = 18KΩ, R_s is found:

$$R_s = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 18 \times 10^3}{100 + 18 \times 10^3} \cong 100\Omega \quad .$$

Then V_{HYS} becomes:

$$V_{HYS} = \frac{100(5.0 - 0.2)}{100 + 18 \times 10^3} = 26.5 \text{ mV}.$$

Therefore, the output of the μA 734 will be 13.25 mV above ground, which is LOW enough as $\overline{\text{TRANSFER}}$ input. A 10 KΩ of offset null potentiometer was added for final calibration. Between pin 14 and V_{cc} of the μA 734, a 5.9 KΩ pull-up resistor was used to insure a + 5.0V HIGH logic level. A capacitor, C_1 (0,047 μF) was added to avoid false triggering.

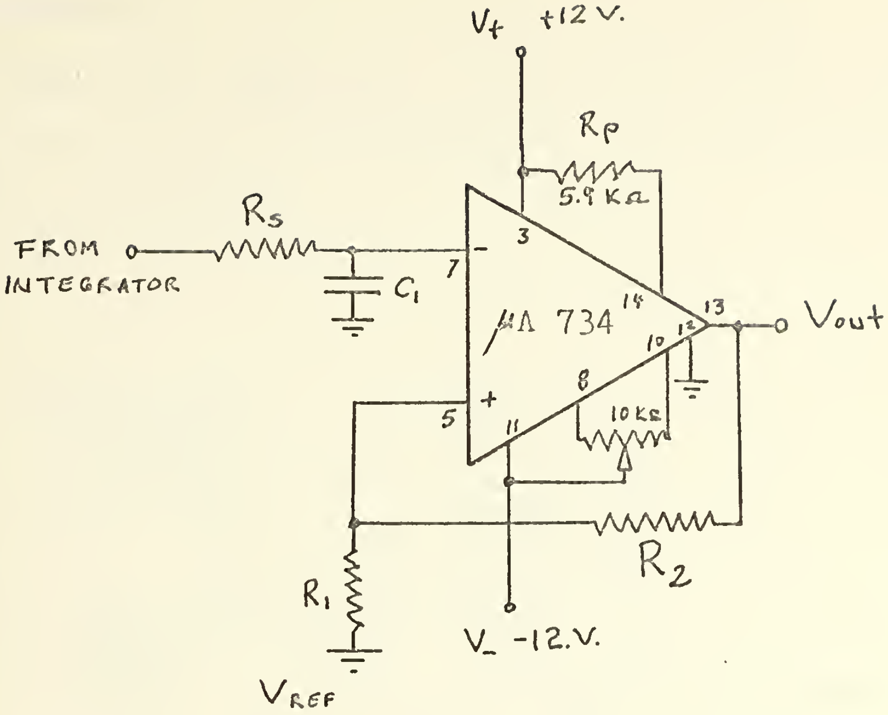


Figure 7. μA 734 Level Sensor Circuit Diagram

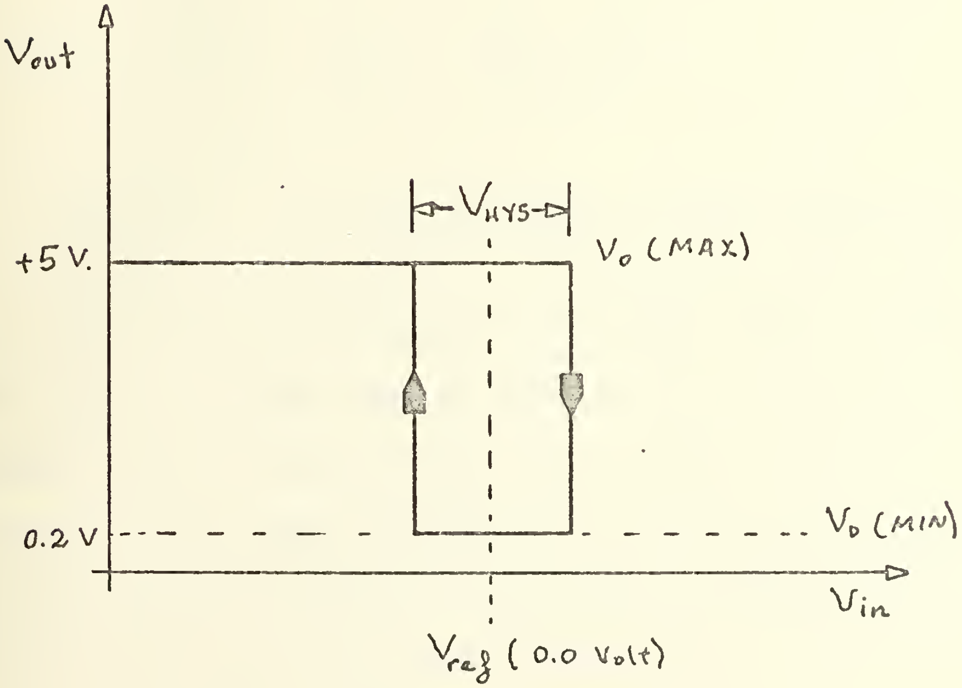


Figure 8. μA 734 Hysteresis Curve

E. INTEGRATOR

A high input impedance, low noise operational amplifier, µA 776 was used for the integrator. The schematic diagram is shown in Figure 9.

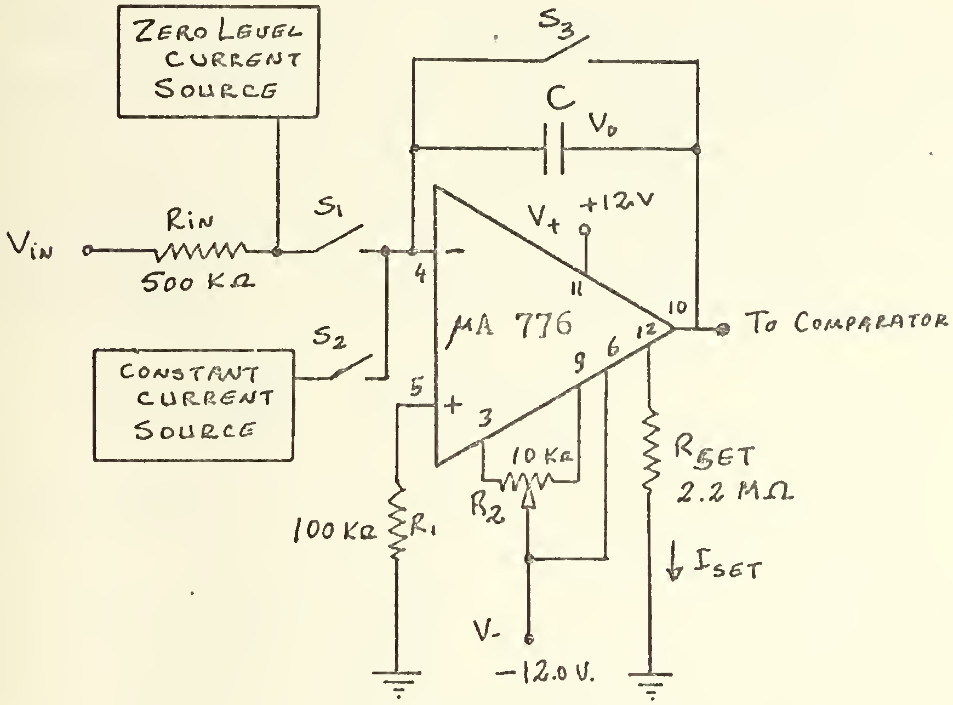


Figure 9. Schematic Diagram of the Integrator

R_2 is the resistor which sets the master bias current (I_{set}). This current defines the parameters of the µA 776 such as: standby supply current, input bias current, input noise voltage (at the input terminals of the µA 776), and the optimum source resistance to be used. A bias current of 5µA was selected from given parameter curves for optimum results. R_{set} is given by:

$$R_{set} = \frac{V_+ - 0.7}{I_{set}}$$

and was calculated as 2.2 MΩ for an I_{set} of 5 μA. An offset null potentiometer (R_2) was added for further adjustment and final calibration.

In the final design, COUNT STATE 20,000 of the 3814 was selected to display 2.000 volts. During COUNT 20,000 to 29,999, S_1, S_2 are OPEN and S_1 is CLOSED. Between 30,000 and 39,999 the unknown current is integrated and the capacitor voltage begins to integrate downwards at the rate

$$\frac{V}{t} = - \frac{V_{in}}{RC} \quad \text{Volt/Second}$$

as found from

$$V_o = - \frac{1}{RC} \int_0^T V_{in} \, dt \tag{8}$$

With the sampling period of 10,000 clock pulses, and a clock frequency of 600 kHz, the integration time was:

$$T = \frac{1}{600 \times 10^3} \times 10{,}000 = 1.667 \times 10^{-2} \text{ seconds}$$

or

$$T = 16.67 \times 10^{-3} \text{ seconds}$$

It was decided that the output voltage of the integrator should be 2.0 volts when the input is 2.0 volts. In this case (8) takes the form:

$$V_o = - \frac{V_{in}}{RC} \times 16.67 \times 10^{-3} \text{ volts}$$

which makes the time constant $RC = 16.67 \times 10^{-3}$ sec.

$R = 500$ KΩ and $C = 0{,}033$ µF was selected for this purpose.

F. CONSTANT CURRENT SOURCE

When the counter reaches 39,999 switch S_1 is opened to remove the unknown voltage from the input of the integrator and switch S_2 is closed to integrate the voltage V_o with a constant slope. Current source in Figure 10 supplies $I_s = 1{,}5$µA for this purpose. A 2MΩ potentiometer was used for final calibration of the circuit.

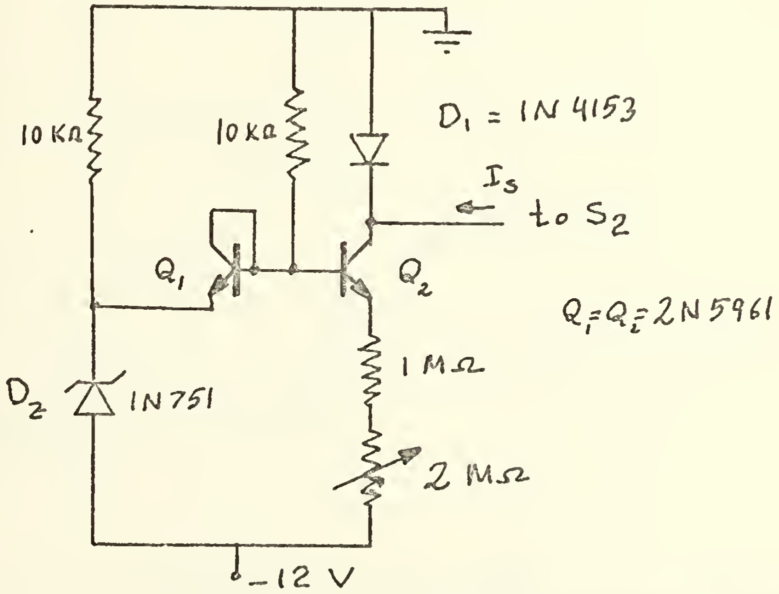


Figure 10. Constant Current Source

G. ZERO OFFSET CIRCUIT

As described in Section IV the counters pause for 10 clock pulses at count 00,000. This pause was used for switching from the input to the current source.

When the input voltage is near or equal to zero volt, the integrator output is close to the null point at the end of its integration. The analog switching glitch causes a false triggering of the comparator. In order to avoid this situation and to allow zero level calibration, another current source offsets the integrator from zero volt. This current source adds a quantity of charge equal to ten counts of I_s to C during the integration of the unknown voltage V_x. This zero offset is shown in Figure 11.

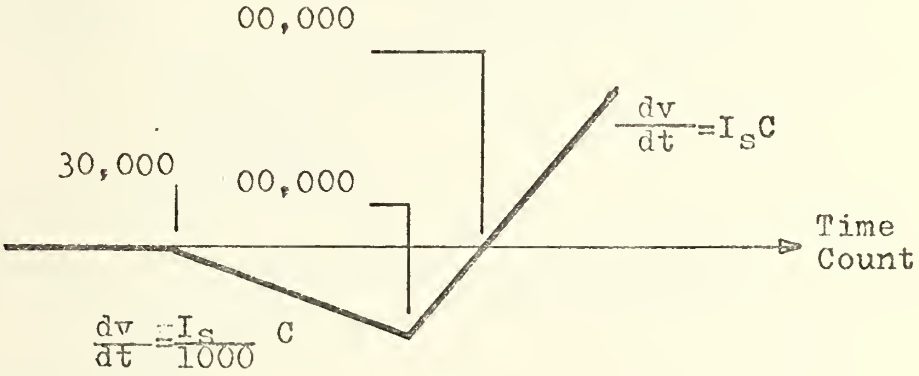


Figure 11. Integrator Output when V_{in} = 0.0 Volt

The circuit which provides this current is given in Figure 12. This fixed offset guarantees that the integrator output moves away from the null even if the input voltage is zero. When the counter on the 3814 reaches 00,000 it remains at zero for ten counts, thus subtracting out the extra ten units of current added during the integration of the unknown voltage.

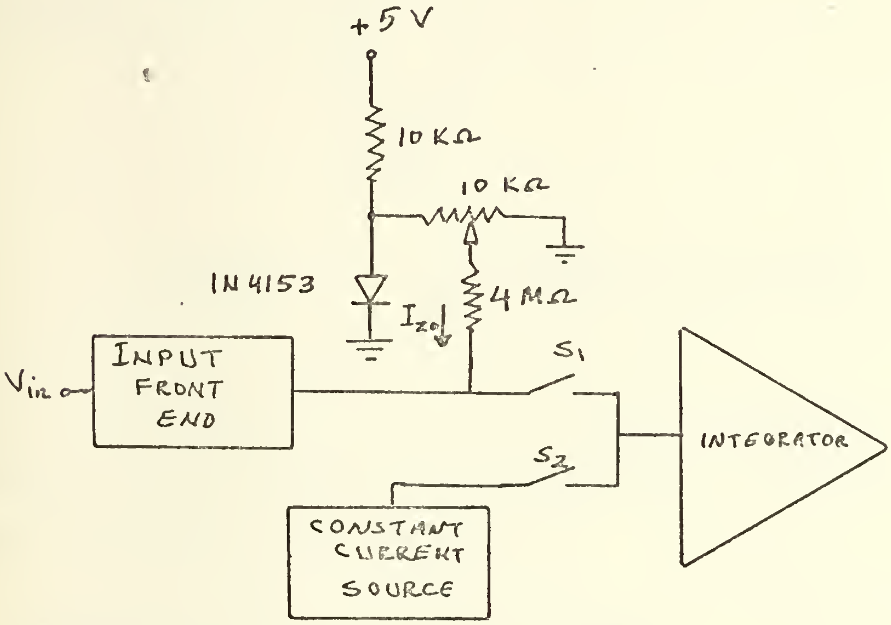


Figure 12. Zero Offset Current Source

H. ANALOG SWITCHES

For S_1, S_2, S_3 and the auto scaling switch S_4, a switch was designed to respond to LOW or HIGH logic levels which are generated by the switching circuits. The analog circuit for this is shown in Figure 13.

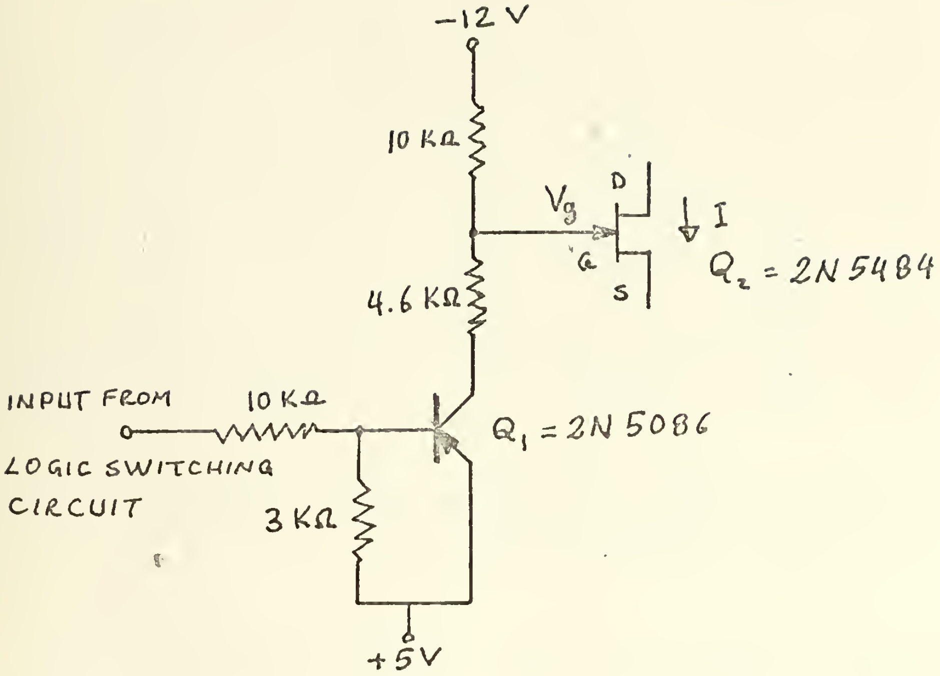


Figure 13. Analog Switching Circuit

When the input is low, Q_1 is ON, and V_g becomes positive turning Q_2 on. When the input is high, both Q_1 and Q_2 are OFF since $V_g = -12.0$ volts.

I. LOGIC CIRCUIT FOR ANALOG SWITCHES

Outputs Q_{E1} and Q_{E2} of the 3814 are used to turn the analog switches ON and OFF at the proper times. The states of the counters, Q_{E1} and Q_{E2}, and the required switch positions are given in Table 2.

	Integrator Switch			Input Sw	Current So.Sw
COUNT	Q_{E1}	Q_{E2}	S_3	S_1	S_2
30,000 to 00,000	1	1	OFF	ON	OFF
00,000 to 10,000	0	0	OFF	OFF	ON
10,000 to 20,000	1	0	OFF	OFF	ON
20,000 to 30,000	0	1	ON	OFF	OFF

Table 2. Analog Switch Positions for a Full Measurement Cycle

To turn a switch ON, a LOW logic level was supplied. Similarly to turn it OFF a high logic level was applied. The required logic circuit is shown in Figure 14.

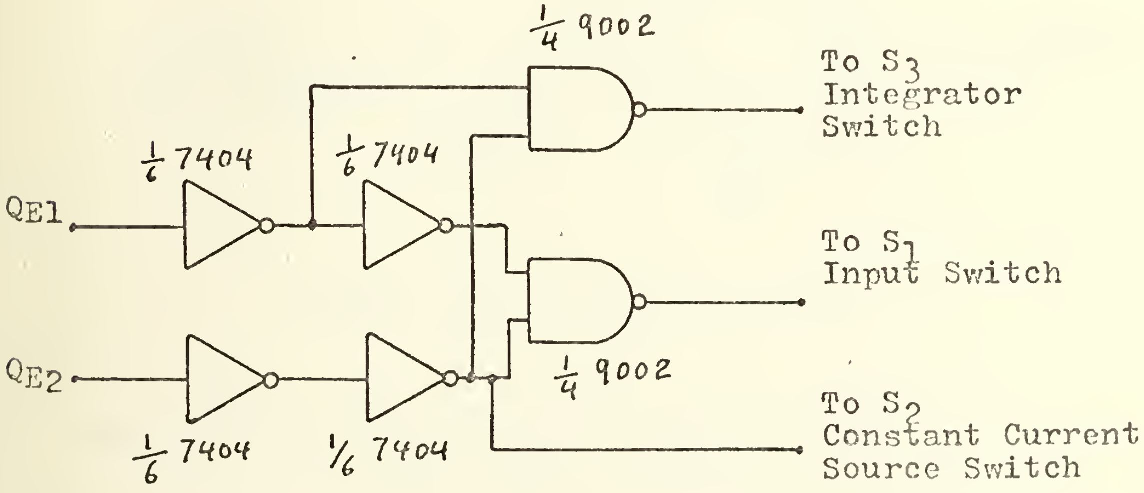


Figure 14. Logic Circuit for S_1, S_2 and S_3

J. OVERRANGE AND UNDERRANGE INDICATORS

1. Overrange Circuit

Up integration of the unknown voltage by the constant current source ends when the counter of the 3814 reaches 19,999 if no TRANSFER command was generated. If a TRANSFER command is generated after a count of 19,999, then the counter state is 20,000 or more and $Q_{E1} = 0$, $Q_{E2} = 1$. This state is decoded and the output is used for the Overrange indicator and as input to the auto ranging circuit. The circuit diagram used for this purpose is shown in Figure 15.

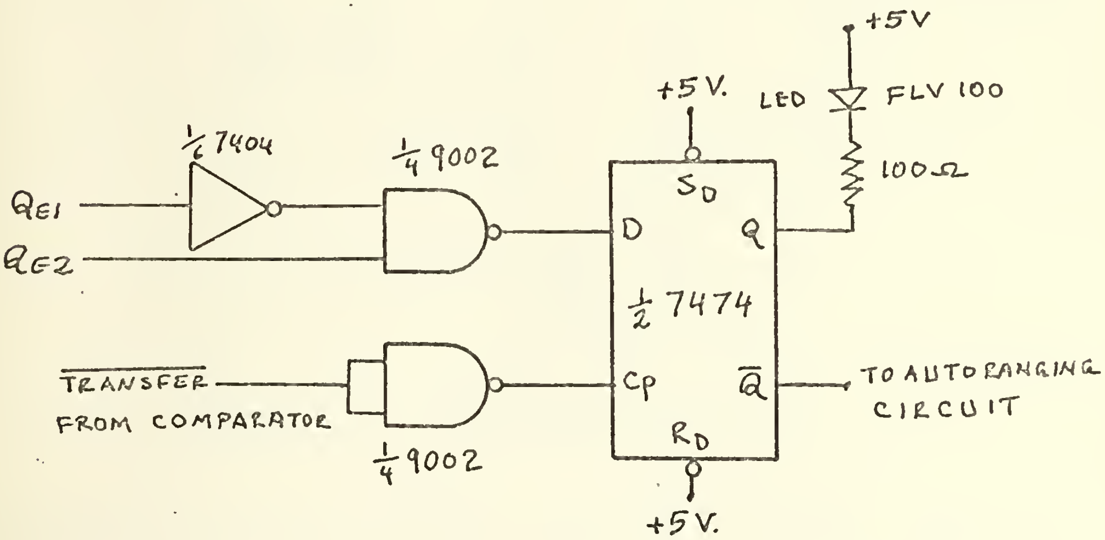


Figure 15. Overrange Circuit

When a TRANSFER command is received while $Q_{E1} = 0$, $Q_{E2} = 1$, Q goes LOW and turns on the LED, indicating an OVERRANGE. $\overline{Q}$ output of the 7474 was used as input to the auto ranging circuit.

2. Underrange Circuit

In order to indicate that the input voltage is less than 10% of full scale and to send a signal to the auto-scaling circuit, an underrange circuit was designed as shown in Figure 16.

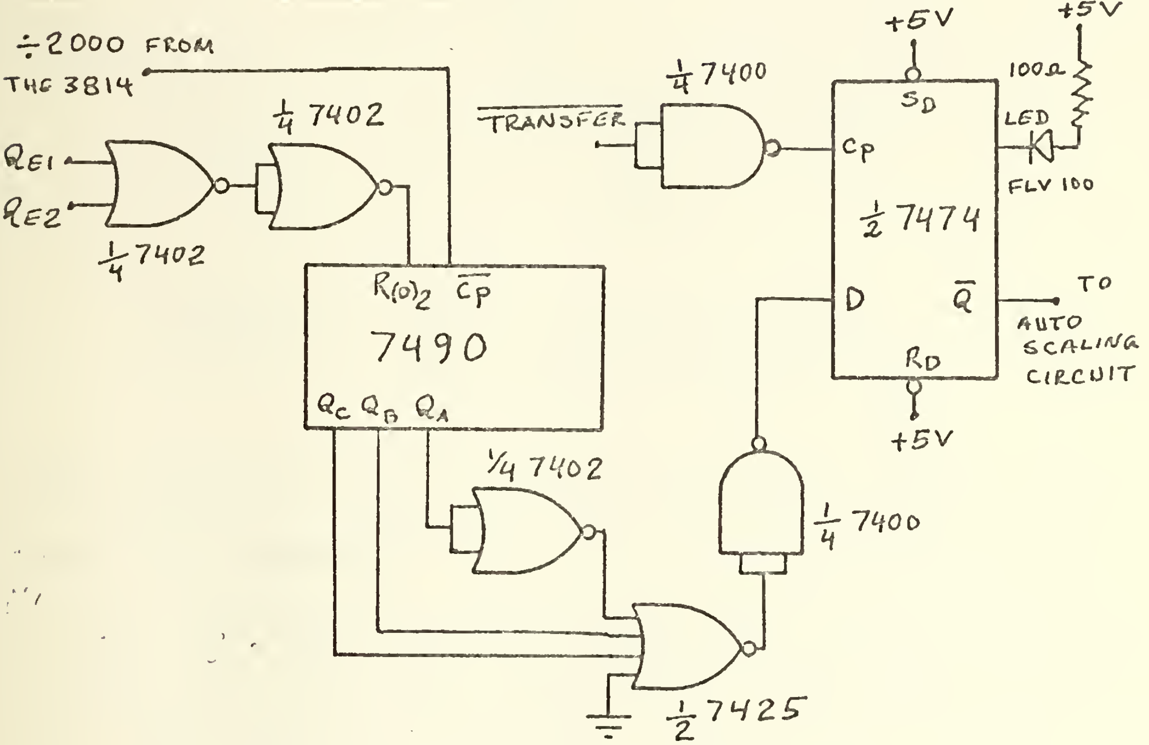


Figure 16. Underrange Indicator

The inputs Q_{E1} and Q_{E2} permit the decade counter 7490 to count during the 00,000 to 10,000 count of the 3814. The "÷ 2000" output was used as CP input for the 7490. Outputs Q_C, Q_B, Q_A of the decade counters were decoded to obtain an underrange pulse as shown in Figure 17.

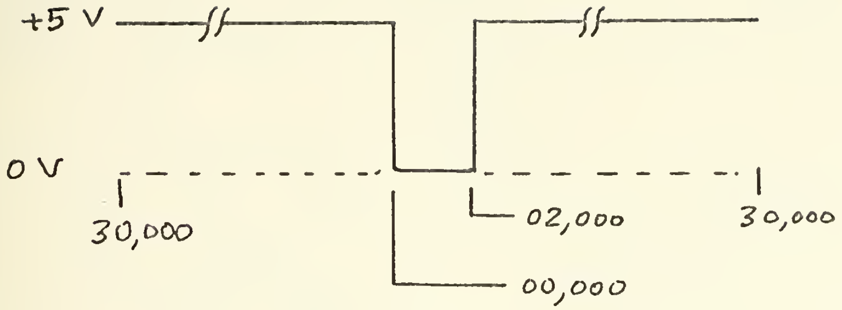


Figure 17. Underrange Pulse During a Full Cycle of the 3814

This underrange pulse was used as "D" input for a D flip-flop. The "TRANSFER" command is used as its clock input. If any "TRANSFER" command occurs during count 00,000 through 02,000 of the 3814, the output of the D flip-flop goes LOW and a LED indicates underrange. The $\overline{Q}$ output of the flip-flop was used as an input to the auto scaling circuit.

K. AUTO - SCALING CIRCUIT

The front end and integrator of the Voltmeter was designed for 0 to +2.0 volts of input voltage.

To change the range from 0 to 2.0 volts and 0 to 20.0 volts, the circuit shown in Figure 18 was designed.

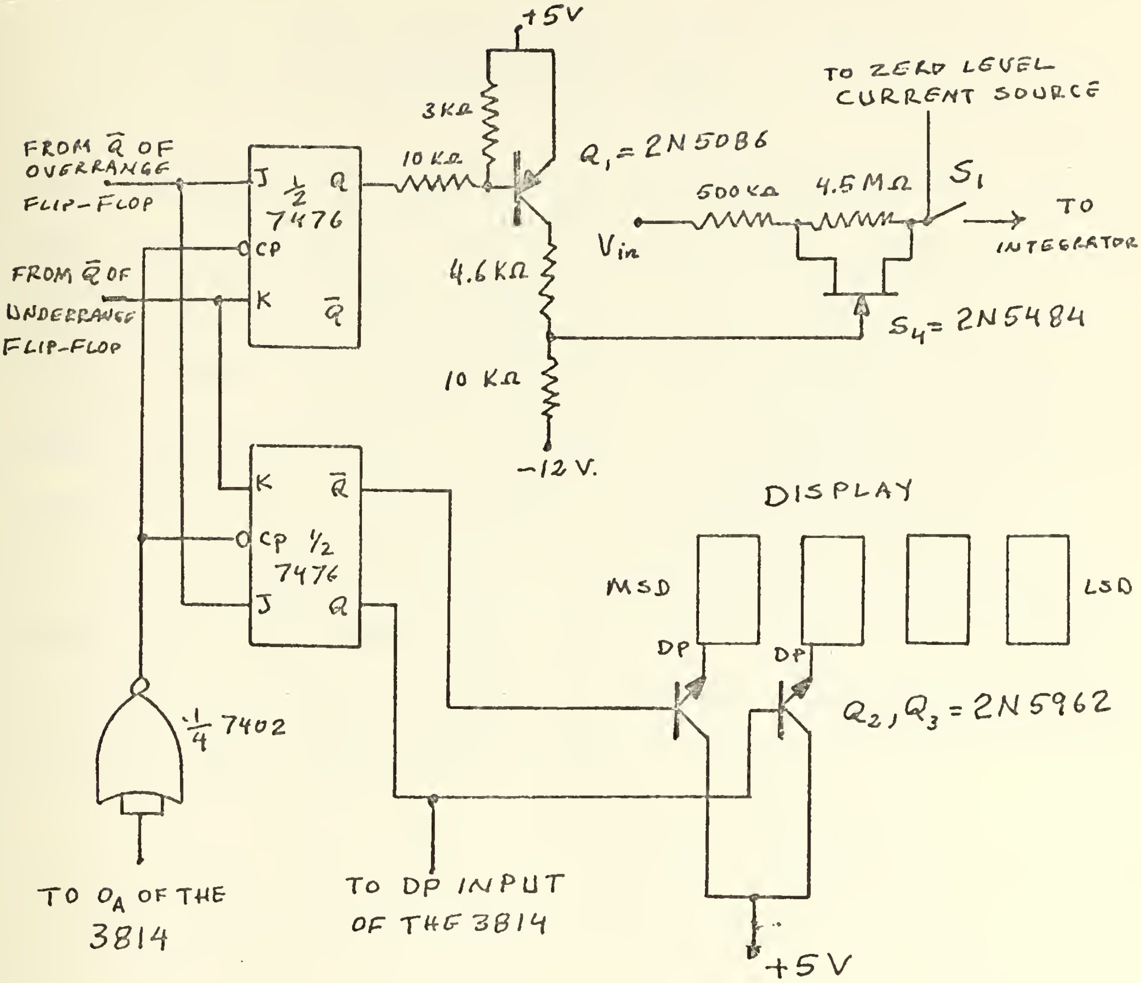


Figure 18. Auto - Scaling Circuit

If at the beginning of each sample cycle, an overrange is present, $\overline{Q}$ goes HIGH, and Q_1 and S_4 are OFF. This connects an additional 4.5 MΩ resistor in series with the input terminals of the voltmeter, introducing a new scaling factor.

In the formula:

$$V_o = \frac{1}{RC} \int_0^T V_{in}\, dt$$

The new R is now 5 MΩ. For 16.67×10^{-3} seconds as before with the input voltage 20.0 volts, the output voltage is:

$$V_o = \frac{20 \times 16.67 \times 10^{-3}}{5 \times 10^{6} \times 0.033 \times 10^{-6}} = 2.0 \text{ volts}$$

which satisfies the requirement of the basic scale. If an underrange occurs, Q_1 and S_4 are turned on, shorting the 4.5 M resistor, and dropping the scale to the 0 to 2.0 volts region. The other half of the 7476 flip-flop in this circuit lights the proper decimal point on the display turning on either Q_2 or Q_3. To suppress a leading zero in the 0 to 20.0 volt range, the state of the decimal point of the second digit was also fed to the "DP" input of the 3814. The unused O_A digit enables the output of the 3814 to be used as clock input to the 7476.

VI. RESULTS AND CONCLUSIONS

The total parts cost was under $100.00. All components were non-precision and commercially available.

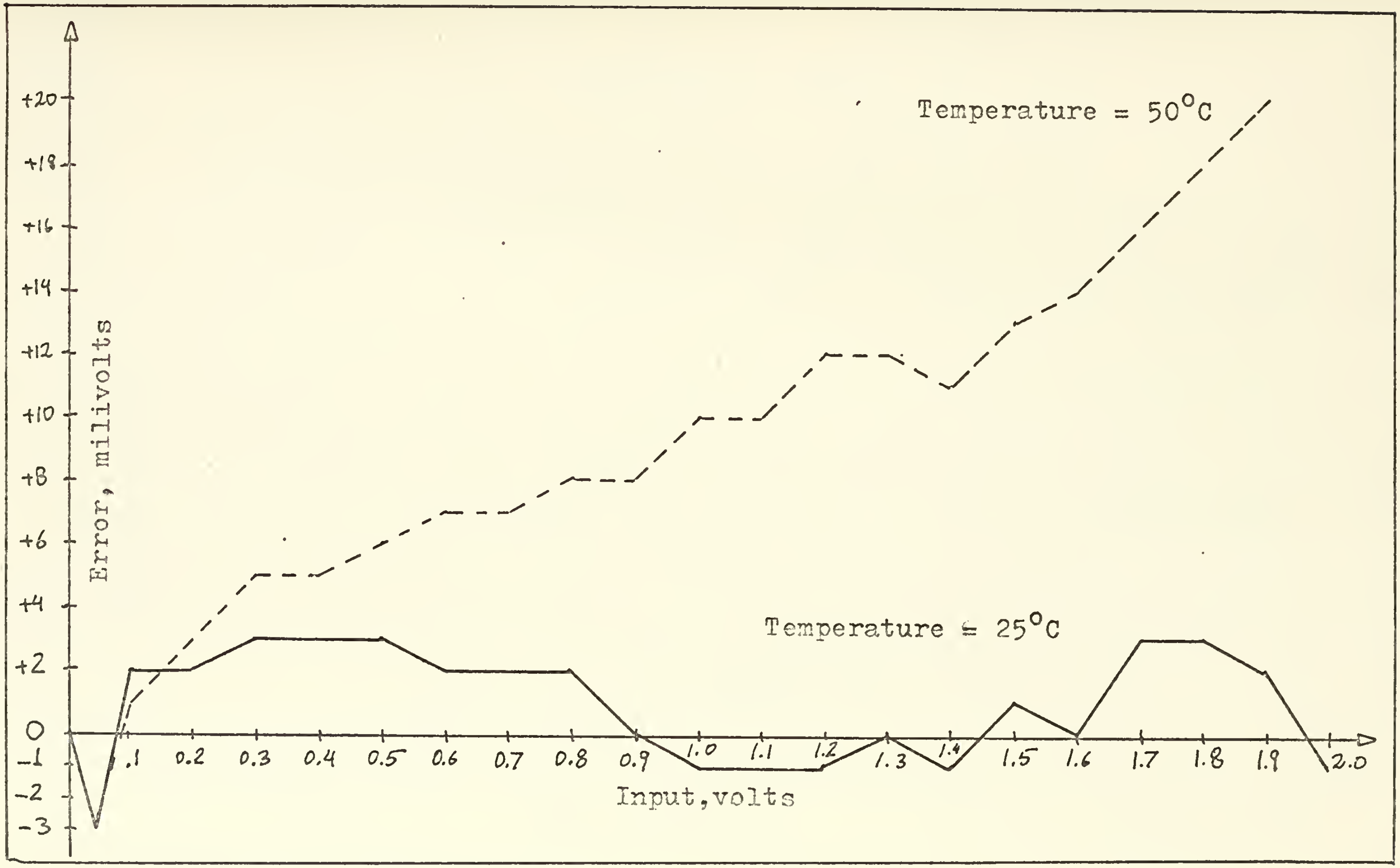
The voltmeter was calibrated and tested against a standard voltage source. Calibration curves are given in Appendix A and Appendix B, the circuit diagram is given in Appendix C, and the connection diagram is given in Appendix D.

At 25°C, the error did not exceed 0.15% of full scale in the 0 to 2.0 volts range and 0.1% in the 2.0 to 20.0 volts range. This error was caused by the non-linearity of the constant current source.

When the temperature was increased to 50°C, the maximum error was found to be 1.2% of full scale. The main cause for this error was the input offset voltage change of the comparator (μA 734). The transfer characteristic of the μA 734 is such that a 100.0μ volt or larger shift of the input voltage changes its output state. At 50°C, the input offset voltage of the comparator shifts by 50.0μ volts from its 25°C null point. The error generated by this temperature increase was found to be more significant than that caused by the constant current source.

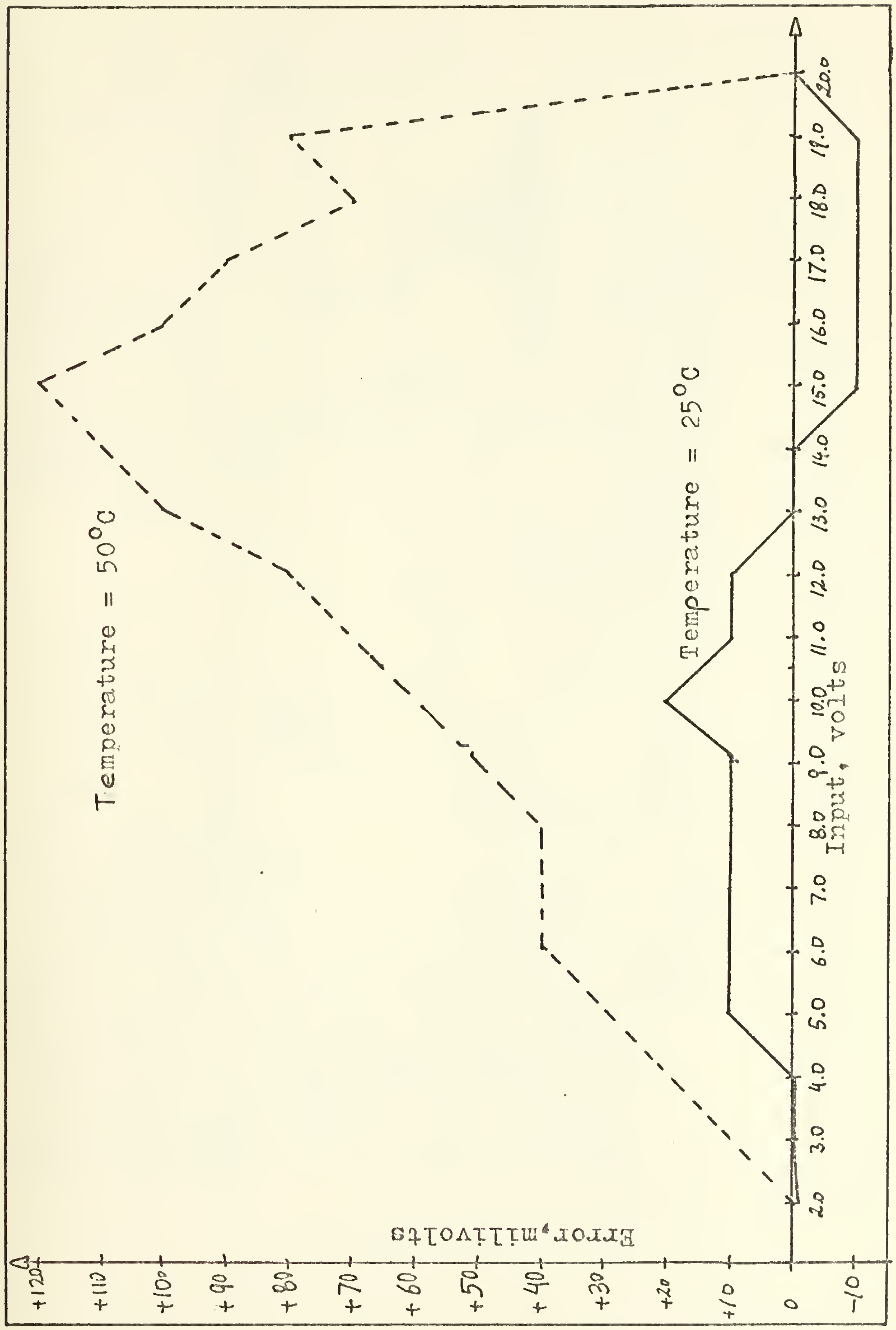
To further improve the accuracy, a temperature compensated constant current source and an improved comparator circuit should be designed.

APPENDIX A



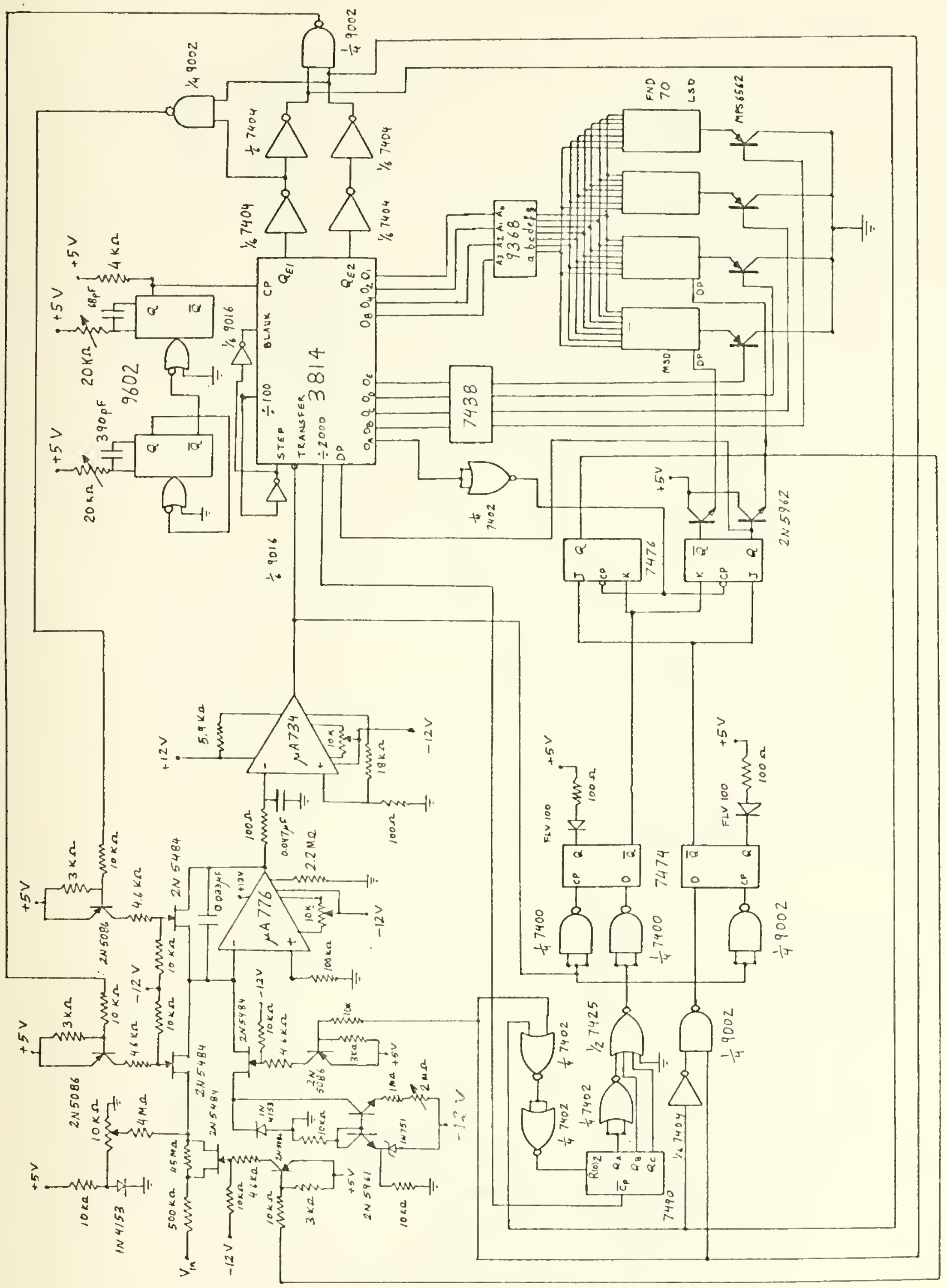
The Error of 0 to 2.0 volts scale

APPENDIX B



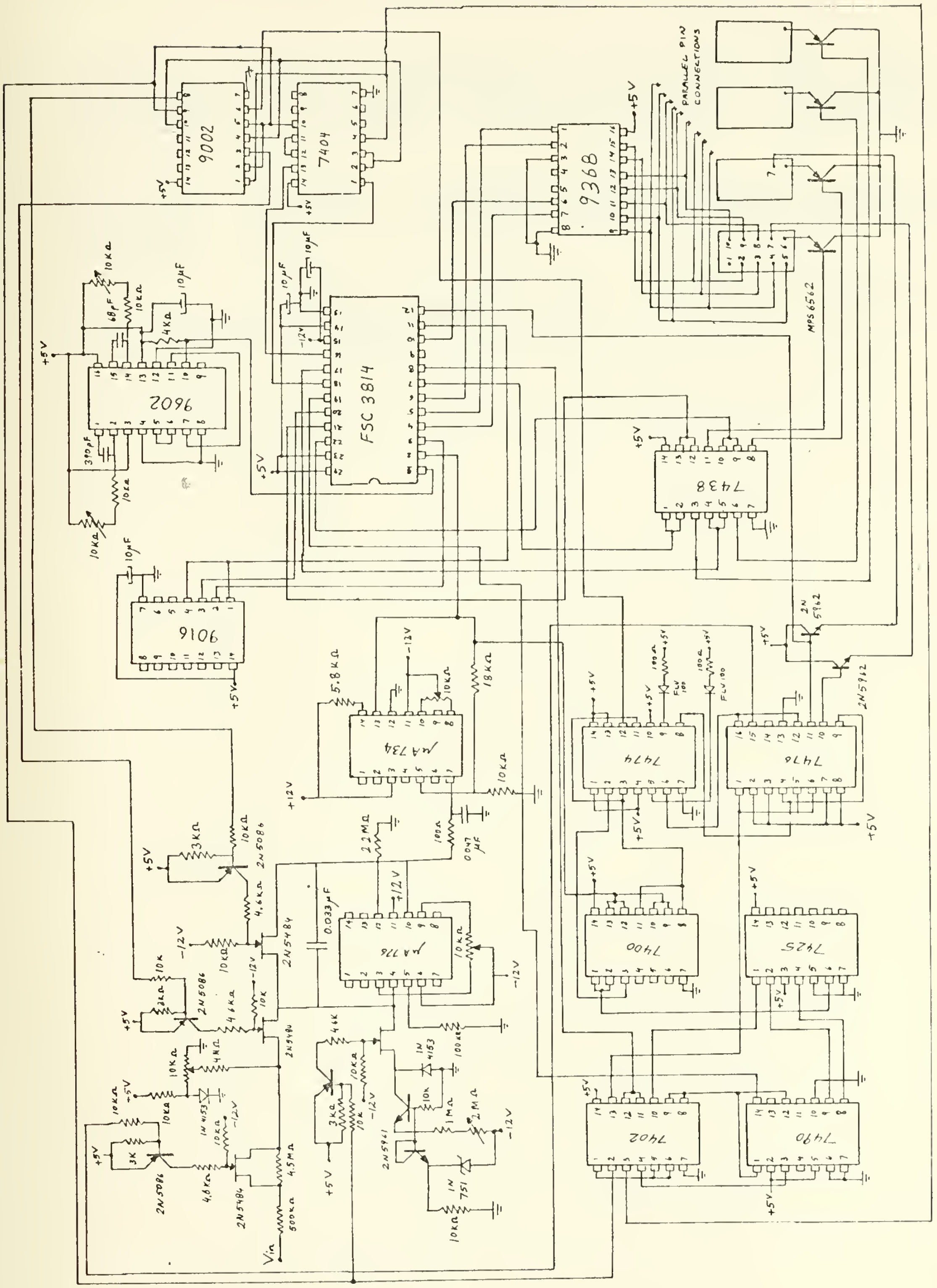
The Error of 2.0 to 20.0 volts scale

APPENDIX C



The Circuit Diagram of the Voltmeter

APPENDIX D



The Connection Diagram of the Voltmeter

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During the past few years, advancement of the integrated circuit technology yielded medium and large scale integration of commonly used electronic circuitry.

One of the special MSI devices commercially available today is the Fairchild 3814 Digital Voltmeter Logic Array which contains most of the logic required for a 4 1/2 decade digital Voltmeter.

In this thesis the design of an inexpensive four digit,

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auto-scaling digital voltmeter is presented with results of tests performed on this meter.

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